|  |  |
| --- | --- |
| **North South University**  Department of Electrical & Computer Engineering    **LAB REPORT**  Course Name: **CSE231L**  Experiment No: 02    Experiment Name:**Universal Gates**  Experiment Date: 15/11/20  Report Submission Date: 21/11/20  Section: 03 | |
| Student Name: **Koushik Banerjee** | Score |
| Student ID: **1812171642** |  |
| Remarks: |

**LAB-02: Universal Gates**

**Objectives:**

* Understand the concept of Universal Gates (NAND & NOR)
* Implement the basic logic gates using universal gates
* Implement Boolean functions using universal gates
* Understand gate level minimization

**Apparatus:**

* Trainer Board
* IC 7400 Quadruple 2-input NAND gates
* IC 7402 Quadruple 2-input NOR gates

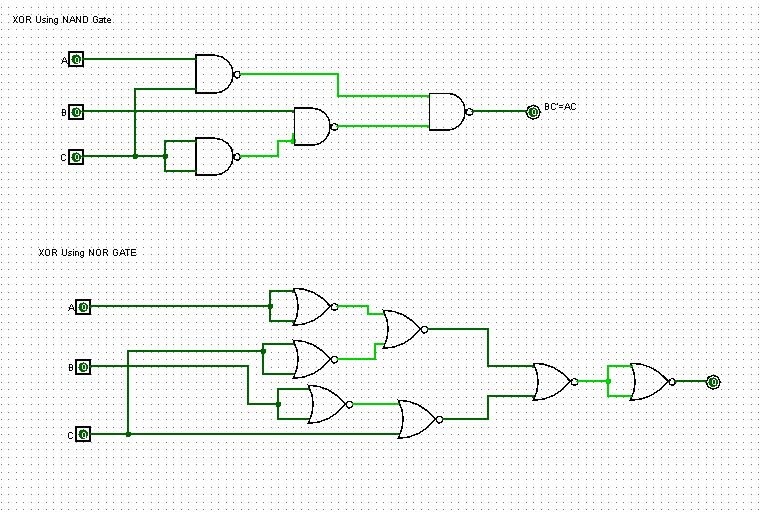
**Theory:**

**Universal Gates:**

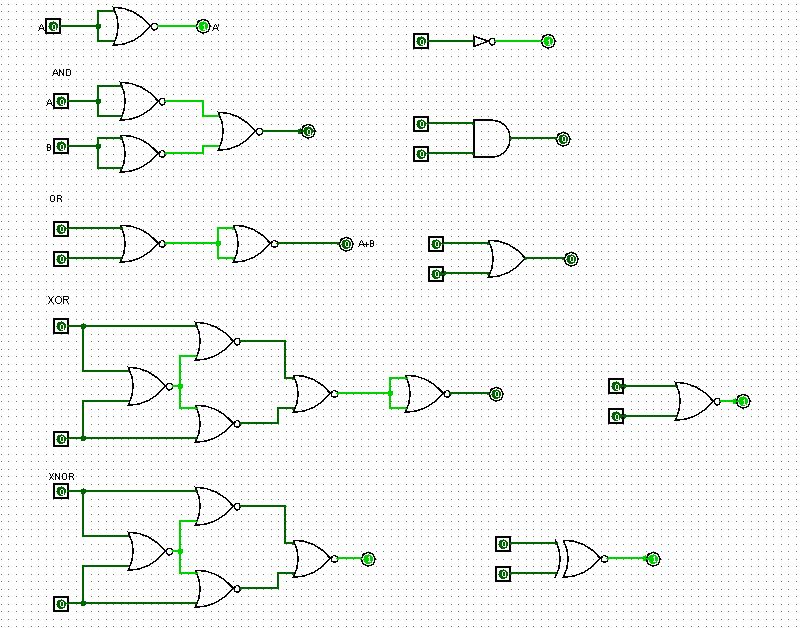
Universal Logic gates can be used to produce any other logic or Boolean function with the NAND and NOR gates being minimal. NAND and NOR gates are called universal gates because they can perform all the three basic logic functions OR, AND and NOT. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. Universal means you can build every possible logic function with all NAND gates or all NOR gates.

**Circuit Diagram:**

**Figure F1: Implementation of XOR and XNOR using NAND gates**



**Figure F2: implementation of NOT, AND, OR, XOR and XNOR using NOR gates**



**Data Table:**

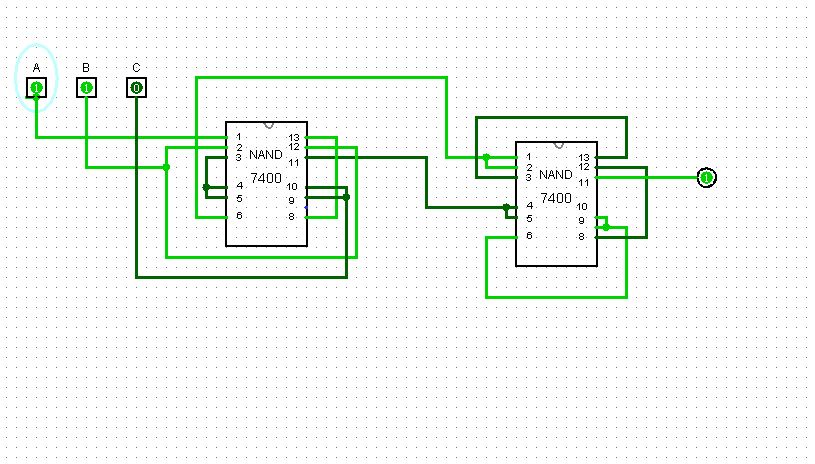
**Table 01: Truth table of the given circuit using universal gates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **I1 = AC** | **I2 = BC’** | **F = I1 + I2** |
| **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **0** | **0** |
| **1** | **0** | **0** | **0** | **0** | **0** |
| **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** | **1** |
| **1** | **1** | **1** | **1** | **0** | **1** |

**Question and Answer:**

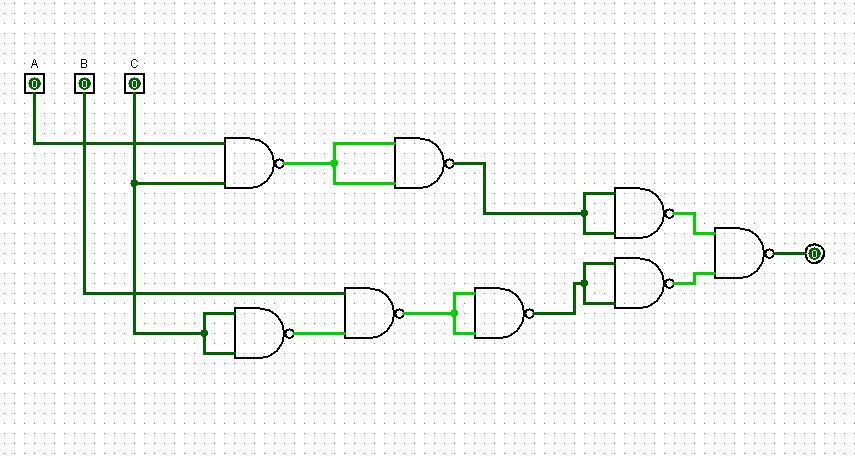
**Answer to Question No. 01:**

IC diagram from the circuit in Figure F3 –Step 2 in Lab Manual



**Answer to Question No. 02:**

Simulation of the circuit in Figure F3 – Step 2 from Lab Manual



**Discussion:**

In lab 2 and in the lab class I face couple of problem doing the IC circuit , I had done mistake on NAND gate IC circuit. There were 2 extra input . I got confused to find out where the problem was. It took some time but finally I found out where the problem was and fix IC circuit and then solved it properly. During the implementation of xor gate using NAND, I also faced some problem there . By the help of our class lab instructor I fix that problem also. That was all human e error problem . After understanding all the problem and practicing that problem, I answered all the questions.